WAVEGUIDE STRESS ENGINEERING AND COMPATIBLE PASSIVATION IN PLANAR LIGHTWAVE CIRCUITS

Abstract of the Disclosure

A planar lightwave circuit includes at least one optical waveguide core, and at least one feature proximate the core having a stress-engineered property to balance stress and therefore minimize birefringence affecting the core. A protective passivation layer is formed over the core and the feature to be substantially non-interfering with the balanced stress provided by the feature. The stress balancing feature may be an overcladding layer formed over the core, doped to have a coefficient of thermal expansion approximately matched to that of an underlying substrate, to symmetrically distribute stress in an undercladding between the overcladding and the substrate, away from the core. The protective passivation layer is formed to have a coefficient of thermal expansion approximately matched to that of the overcladding. In one exemplary embodiment, the passivation layer is formed from silicon nitride. Related concepts of stress release grooves, and core overetching, are also disclosed.